



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,231	10/19/2001	Stephen J. Sicola	P01-3673	7807

22879 7590 01/09/2004

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER

PATEL, NIKETA I

ART UNIT	PAPER NUMBER
----------	--------------

2182

DATE MAILED: 01/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/038,231

Applicant(s)

SICOLA ET AL.

Examiner

Niketa I. Patel

Art Unit

2182

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 October 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 October 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4, 5. 6) ☐ Other: _____

Art Unit: 2182

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- a. The term "***substantially***" in claim 8 is a relative term which renders the claim indefinite. The term "***substantially***" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. It is unclear as to what extent the first junction box and the second junction box are to each other.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

Art Unit: 2182

A person shall be entitled to a patent unless -

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 7-13, 15-17 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Martinez et al. U.S. Patent

Number: 5,790,782 (hereinafter referred to as "Martinez".)

5. **Referring to claim 1**, Martinez teaches a position sensing apparatus for use in a data storage cabinet having multiple shelves for receiving device enclosures [see column 1 - lines 38-49], comprising: a first junction box having an output connection at a first shelf of the cabinet for providing a first shelf identifier signal to a device enclosure connected to the first shelf [see figure 1 - element 15; column 4 - lines 8-33, 'connector']; and a second junction box linked to the first junction box [see figure 1 - element 15, 16, 17] for receiving an output signal and having an output connection at a second shelf of the cabinet for providing a second shelf identifier signal to a device enclosure connected to the second shelf, wherein the second shelf identifier signal differs from the first shelf identifier signal [see column 1 - lines 55-60; column 2 - lines 33-44; see figure 6 - element 17; column 5 - lines 39-57.]

Art Unit: 2182

6. **Referring to claim 2**, *Martinez* teaches that the first and second junction boxes each include an additional output connection at third and fourth shelves of the cabinet for providing third and fourth shelves of the cabinet for providing third and fourth shelf identifier signals differing from the first and second shelf identifier signals, respectively [see figure 1 - element 11, 16, 15, 12-14; column 2 - lines 33-44; column 5 - lines 39-57.]

7. **Referring to claim 3**, *Martinez* teaches that each of the junction boxes includes a sensing wire providing signals to the output connections and being alternately grounded and open to differentiate the first and second shelf identifier signals from the third and fourth shelf identifier signals [see figure 6 - element 43, 35.]

8. **Referring to claim 4**, *Martinez* teaches that the junction boxes include a first and a second set of sensing wires each providing a number of bit signals that are included in the shelf identifier signals to the output connections [see figure 6 - elements 38, 37, 41, 44.]

9. **Referring to claim 7**, *Martinez* teaches that the sensing wires of the first and second sets are passed through the first junction box and are included in the output signal to the second junction box and further wherein each of the sensing wires in

Art Unit: 2182

the first set are moved one position within the first set and each of the sending wires in the second set are moved one position within the second set prior to the link with the second junction box [see column 5 - lines 39-67; column 6 - lines 1-34.]

10. **Referring to claim 8**, *Martinez* teaches that the first junction box and the second junction box are *substantially* identical and interchangeable [see figure 1 - elements 15, 16.]

11. **Referring to claim 9**, *Martinez* teaches that including a cabinet area network bus having terminating resistors at each end [see figure 6 - elements 43, 35, 'resisters'.]

12. **Referring to claim 10**, *Martinez* teaches a cabinet for physically storing and communicatively linking computing devices, comprising: a plurality of shelves adapted for receiving device enclosures [see figure 1 - elements 1-4]; a cabinet bus linked to each of the shelves and adapted to provide a unique shelf identifier signal to each of the shelves [see figure 1 - element 17, 18; column 1 - lines 55-60; column 2 - lines 33-44; see figure 6 - element 17; column 5 - lines 39-57]; and means for providing information identifying the cabinet to each of the shelves [see figure 1 - element 19, 18.]

13. **Referring to claim 11**, *Martinez* teaches further including a device enclosure on one of the shelves comprising processor for

Art Unit: 2182

processing the unique shelf identifier to determine a physical location within the cabinet [see column 5 - lines 28-44, 'EMU'.]

14. **Referring to claim 12**, *Martinez* teaches that the processor includes the determined physical location and the cabinet identification information in message transmitted outside the enclosure [see column 5 - lines 28-67; column 6 - lines 1-31.]

15. **Referring to claim 13**, *Martinez* teaches that the processor determines the physical location by retrieving a shelf identifier from memory using the received shelf identifier signal [see column 1 - lines 64-67; column 2 - lines 1-34; column 5 - lines 65-67.]

16. **Referring to claim 15**, *Martinez* teaches that the cabinet bus comprises a plurality of serially connected junction boxes each including a first set of sensing and a second set of sensing wires and a side connector linked to one of the shelves for providing the shelf identifier signal from the first and second sets of sensing wires [see figure 1 - elements 15, 16, 17, 11-14.]

17. **Referring to claim 16**, *Martinez* teaches that each of the sensing wires in the first set are moved one position and each of the sensing wires in the second set are moved one position prior to the connection to an adjacent junction box to provide an output signal to modify the shelf identifier signal in each

Art Unit: 2182

consecutive junction box in the cabinet bus [see column 5 - lines 28-67; column 6 - lines 1-31.]

18. **Referring to claim 17**, Martinez teaches that each junction box further includes an additional side connector linked to the first and second sets of sensing wires and an additional sensing wire that is linked to the side connectors and is alternately grounded and ungrounded at each side connector to provide differing one of the shelf identifier signals within each junction box [see figure 6 - elements 35, 43; column 5 - lines 28-67; column 6 - lines 1-31.]

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

20. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered

Art Unit: 2182

therein were made absent any evidence to the contrary.

Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

21. Claim 5-6, 14, 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martinez et al. U.S. Patent Number: 5,790,782 (hereinafter referred to as "*Martinez*".)

22. **Referring to claim 14**, *Martinez* teaches that the received shelf identifier signal is a 5-bit signal, however fails to teach that the received shelf identifier signal is an 8-bit signal. *Martinez* discloses that the 5-bit signal is an example, not to be taken as a limitation on the spirit and scope of this invention [see column 9 - lines 15-23.]

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention that it was old and well known in the computer art to get the advantage of being able to address greater number of elements with a higher bit signal. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to include a higher bit signal to get this advantage.

Art Unit: 2182

23. **Referring to claim 19**, Martinez teaches a data storage system with passive position determination of enclosures, comprising: a cabinet having a plurality of shelves for receiving and linking computing devices [see figure 1 - elements 1-4], a cabinet bus linked to the shelves for providing a shelf identifier to each shelf [see figure 1 - element 17], and a device for providing a cabinet identifier to each shelf [see figure 1 - elements 15, 16]; a device enclosure positioned on one of the shelves in one of the cabinets and linked to the cabinet bus in the one cabinet, wherein the device enclosure receives the shelf identifier for the one shelf and the cabinet identifier for the one cabinet and creates and transmits a physical location message [see column 1 - lines 55-67; column 2 - lines 1-44]; and a host linked to the one cabinet receiving the physical location message and outputting a physical location of the device enclosure including the one shelf and the one cabinet [see figure 5 - element 30], however fails to teach a plurality of cabinets containing above elements.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention that it was old and well known in the computer art to get the advantage of having plurality of storage locations to hold multiple enclosures by using plurality of cabinets. It would have been obvious to one

Art Unit: 2182

of ordinary skill in the art at the time of applicant's invention to include a plurality of cabinets to get this advantage.

24. **Referring to claim 20**, *Martinez* teaches that the cabinet bus includes a plurality of junction boxes comprising a first and second set of sensing wires linked to the shelves and carrying the shelf identifier [see figure 1 - elements 15, 16], the sensing wires of the first set rotating one position within the first set prior to connection to the next one of the junction boxes and the sensing wires of the second set rotating one position within the second set prior to connection to the next one of the junction boxes, whereby the shelf identifier output to the next one of the junction boxes is modified [see column 5 - lines 28-67; column 6 - lines 1-31.]

25. **Referring to claim 21**, *Martinez* teaches that each of the junction boxes is connected to two shelves and the cabinet bus further includes an additional sensing line that is grounded prior to a first one of the two shelves and is ungrounded prior to a second one of the two shelves [see figure 1 - elements 15, 16, 17, 11-14; figure 6 - element 35, 43; column 6 - lines 47-59.]

26. **Referring to claims 5-6 and 18**, *Martinez* teaches that the number of signals is based on the number of wires in each of the

Art Unit: 2182

sets [see column 5 - lines 40-57] however, fails to teach that the number of wires in the first set differs from the number in the second set and that the number of wires in the first set is three and the number of wires in the second set is four, to provide at least 24 of the unique shelf identifier signals wires to provide at least 24 of the unique shelf identifier signals within the cabinet bus.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention that it was old and well known in the computer art to get the advantage of being able to address grater number of elements with a higher bit signal and lesser number of elements with a smaller bit signal. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to include a higher/smaller bit signal to get this advantage.

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following documents have been made record of to further show the state of the art as it pertains to multi-self cabinet with a capability of determining physical location of each of the shelves.

Martinez et al. U.S. Patent Number: 5,956,665

Art Unit: 2182

Martinez et al. U.S. Patent Number: 5,892,973

Mizuno et al. U.S. Patent Number: 5,838,891

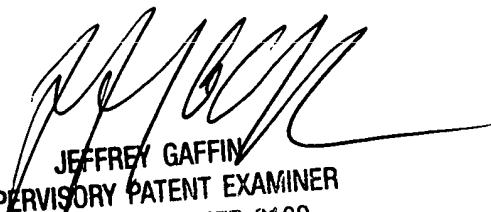
Bleiweiss et al. U.S. Patent Number: 5,901,151

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Niketa I. Patel whose telephone number is (703) 305 4893. The examiner can normally be reached on M-F 8:00 A.M. to 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A. Gaffin can be reached on (703) 308 3301. The fax phone number for the organization where this application or proceeding is assigned is (703) 872 9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305 3900.

NP
1/6/2003


JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100